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\* Design Summary \*

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Top Level Output File Name : incrementer.ngc

Primitive and Black Box Usage:

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# BELS : 96

# GND : 1

# INV : 1

# LUT1 : 30

# MUXCY : 31

# VCC : 1

# XORCY : 32

# IO Buffers : 64

# IBUF : 32

# OBUF : 32

Device utilization summary:

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Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 31 out of 5720 0%

Number used as Logic: 31 out of 5720 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 31

Number with an unused Flip Flop: 31 out of 31 100%

Number with an unused LUT: 0 out of 31 0%

Number of fully used LUT-FF pairs: 0 out of 31 0%

Number of unique control sets: 0

IO Utilization:

Number of IOs: 64

Number of bonded IOBs: 64 out of 102 62%

Specific Feature Utilization:

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 6.079ns

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis

Total number of paths / destination ports: 528 / 32

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Delay: 6.079ns (Levels of Logic = 35)

Source: in<0> (PAD)

Destination: in\_plus<31> (PAD)

Data Path: in<0> to in\_plus<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 1 1.222 0.579 in\_0\_IBUF (in\_0\_IBUF)

INV:I->O 1 0.206 0.000 Madd\_in\_plus\_lut<0>\_INV\_0 (Madd\_in\_plus\_lut<0>)

MUXCY:S->O 1 0.172 0.000 Madd\_in\_plus\_cy<0> (Madd\_in\_plus\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<1> (Madd\_in\_plus\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<2> (Madd\_in\_plus\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<3> (Madd\_in\_plus\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<4> (Madd\_in\_plus\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<5> (Madd\_in\_plus\_cy<5>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<6> (Madd\_in\_plus\_cy<6>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<7> (Madd\_in\_plus\_cy<7>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<8> (Madd\_in\_plus\_cy<8>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<9> (Madd\_in\_plus\_cy<9>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<10> (Madd\_in\_plus\_cy<10>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<11> (Madd\_in\_plus\_cy<11>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<12> (Madd\_in\_plus\_cy<12>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<13> (Madd\_in\_plus\_cy<13>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<14> (Madd\_in\_plus\_cy<14>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<15> (Madd\_in\_plus\_cy<15>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<16> (Madd\_in\_plus\_cy<16>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<17> (Madd\_in\_plus\_cy<17>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<18> (Madd\_in\_plus\_cy<18>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<19> (Madd\_in\_plus\_cy<19>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<20> (Madd\_in\_plus\_cy<20>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<21> (Madd\_in\_plus\_cy<21>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<22> (Madd\_in\_plus\_cy<22>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<23> (Madd\_in\_plus\_cy<23>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<24> (Madd\_in\_plus\_cy<24>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<25> (Madd\_in\_plus\_cy<25>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<26> (Madd\_in\_plus\_cy<26>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<27> (Madd\_in\_plus\_cy<27>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<28> (Madd\_in\_plus\_cy<28>)

MUXCY:CI->O 1 0.019 0.000 Madd\_in\_plus\_cy<29> (Madd\_in\_plus\_cy<29>)

MUXCY:CI->O 0 0.019 0.000 Madd\_in\_plus\_cy<30> (Madd\_in\_plus\_cy<30>)

XORCY:CI->O 1 0.180 0.579 Madd\_in\_plus\_xor<31> (in\_plus\_31\_OBUF)

OBUF:I->O 2.571 in\_plus\_31\_OBUF (in\_plus<31>)

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Total 6.079ns (4.921ns logic, 1.158ns route)

(81.0% logic, 19.0% route)

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Cross Clock Domains Report:

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Total REAL time to Xst completion: 7.00 secs

Total CPU time to Xst completion: 6.95 secs

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Total memory usage is 4506632 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)